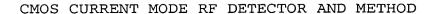
5



## Abstract of the Disclosure

An integrated detector circuit (20) includes first and second gain stages ( $GS_1$ ,  $GS_2$ ). The first gain stage has an input (82) that monitors a high frequency signal ( $V_{RFDET}$ ) for routing a first detection current ( $IS_1$ ) to a node (60). The second gain stage includes a first current source ( $PF_1$ ) that supplies a bias current ( $I_{MAX1}$ ) indicative of a predefined amplitude of the high frequency signal. An input of the second gain stage monitors the high frequency signal to route a portion of the bias current to the node as a second detection current ( $IS_2$ ), which is limited to the bias current when the high frequency signal is greater than the predefined amplitude to compensate for a nonlinearity in a transconductance of the second gain stage.